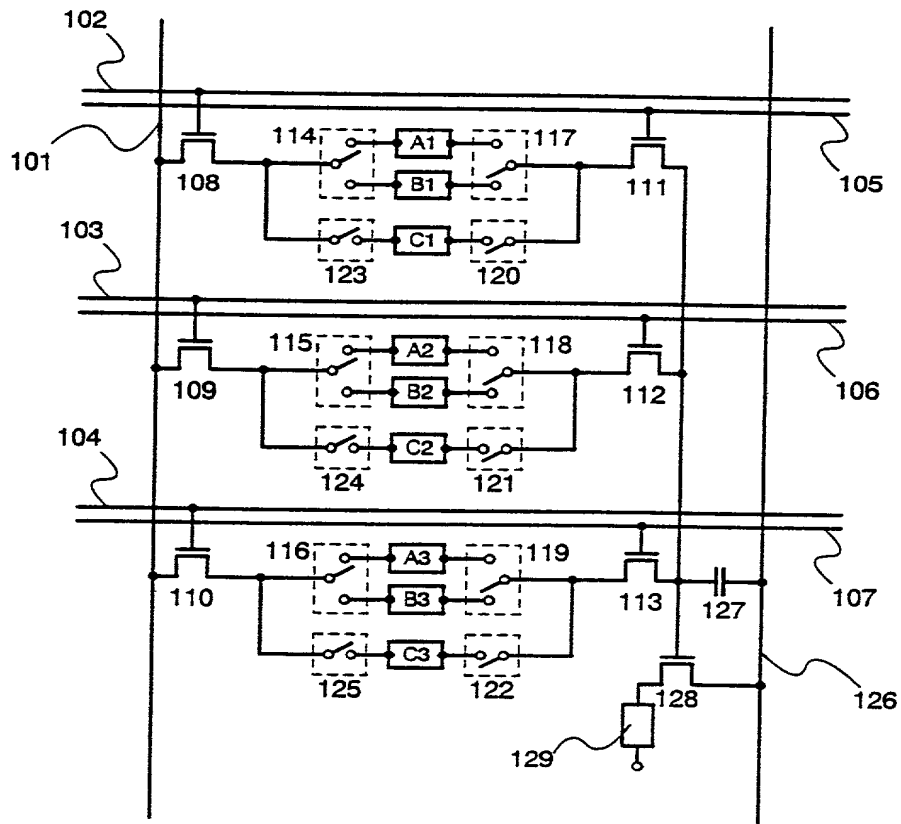


Fig. 1



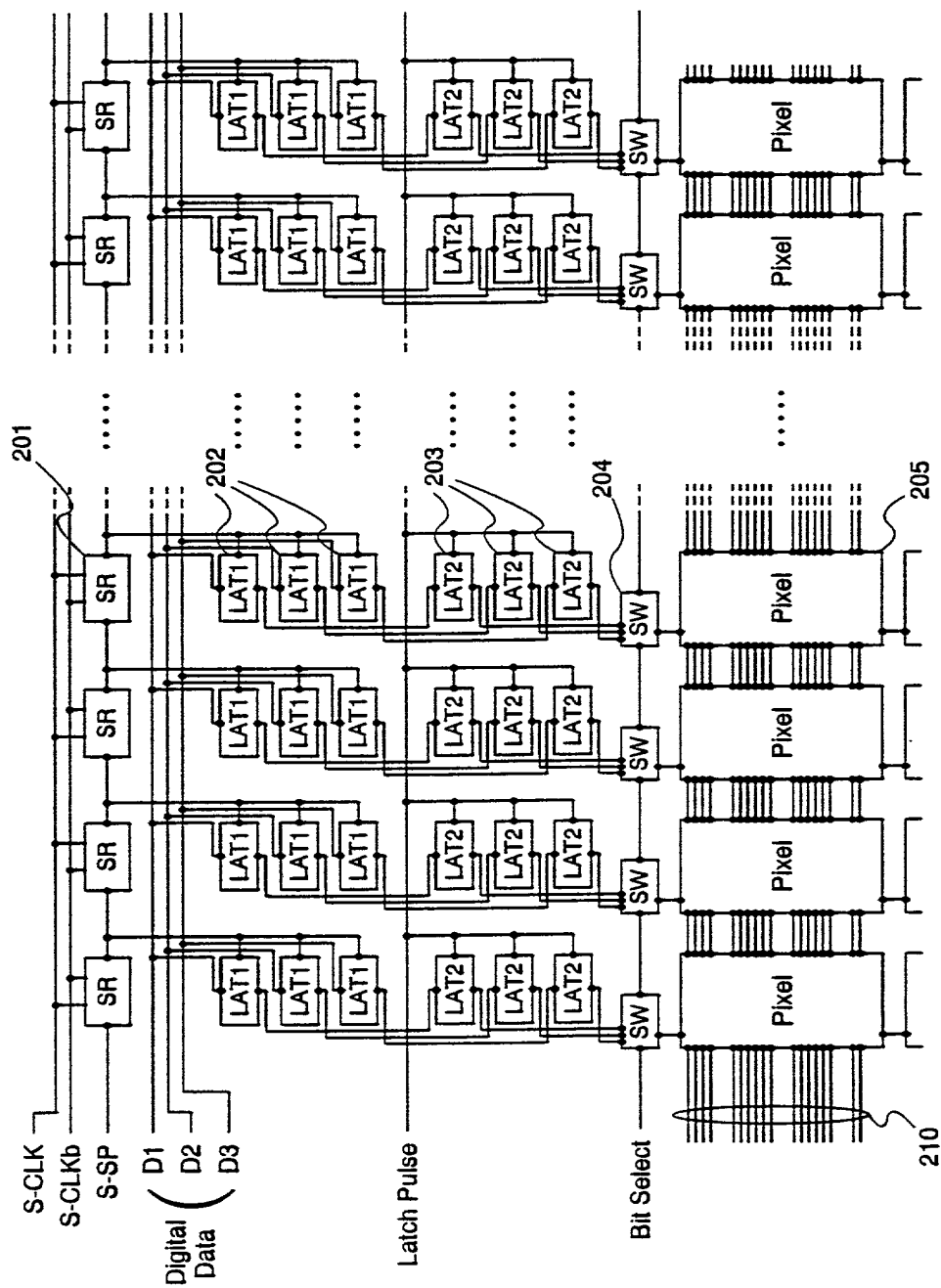
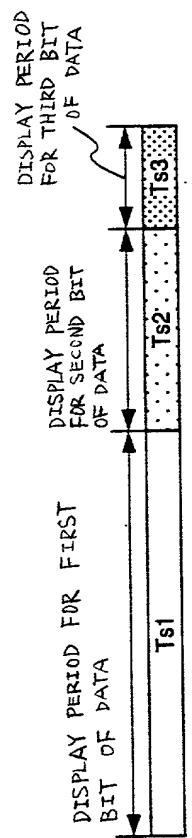
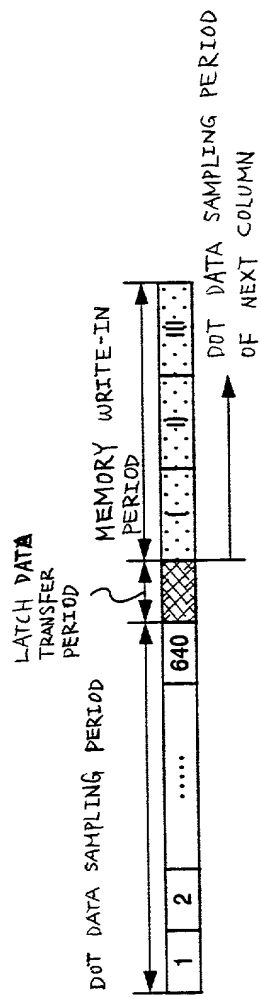
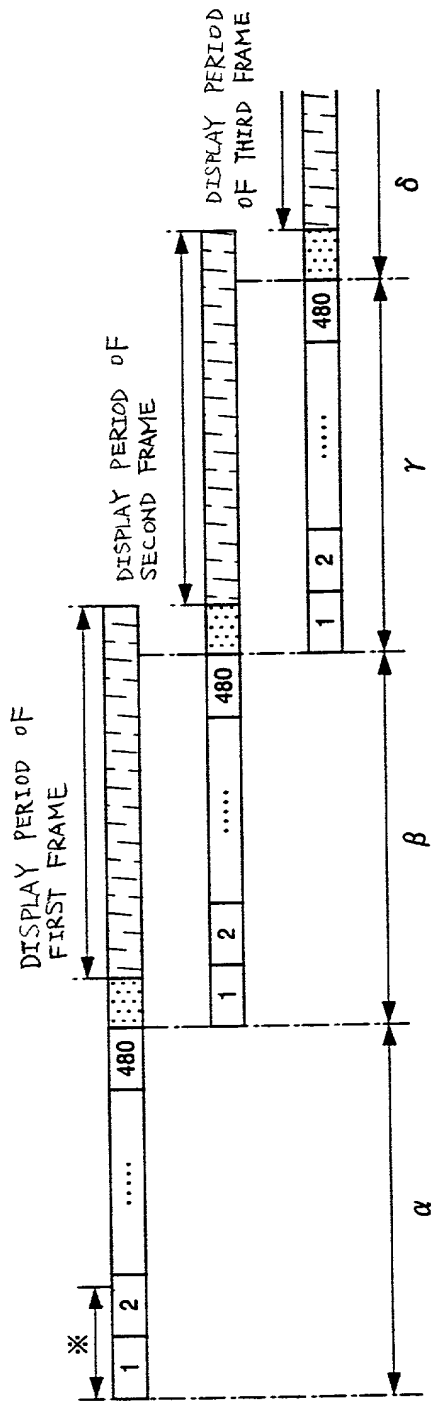
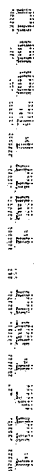


Fig. 2



[illegible]

401 : SOURCE SIGNAL LINE
444 : STORAGE CAPACITOR (C_s)
445 : EL DRIVER TFT (NV)

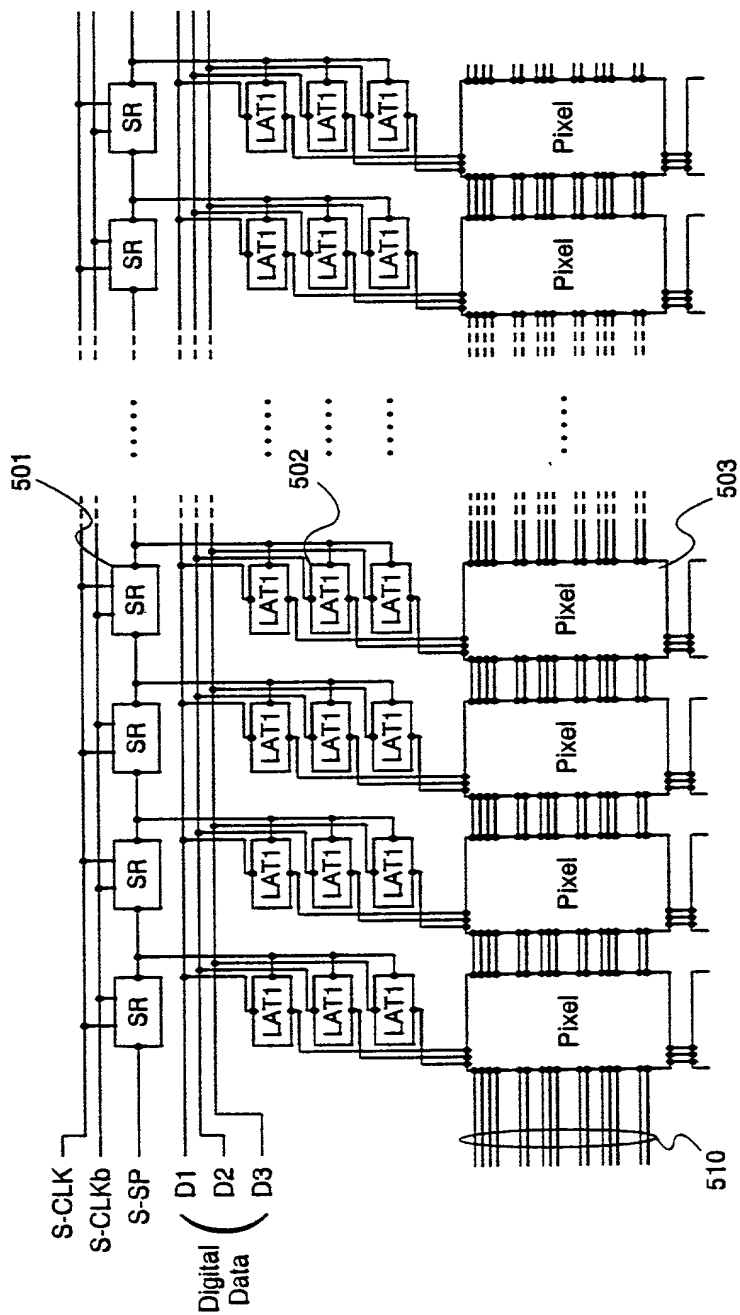
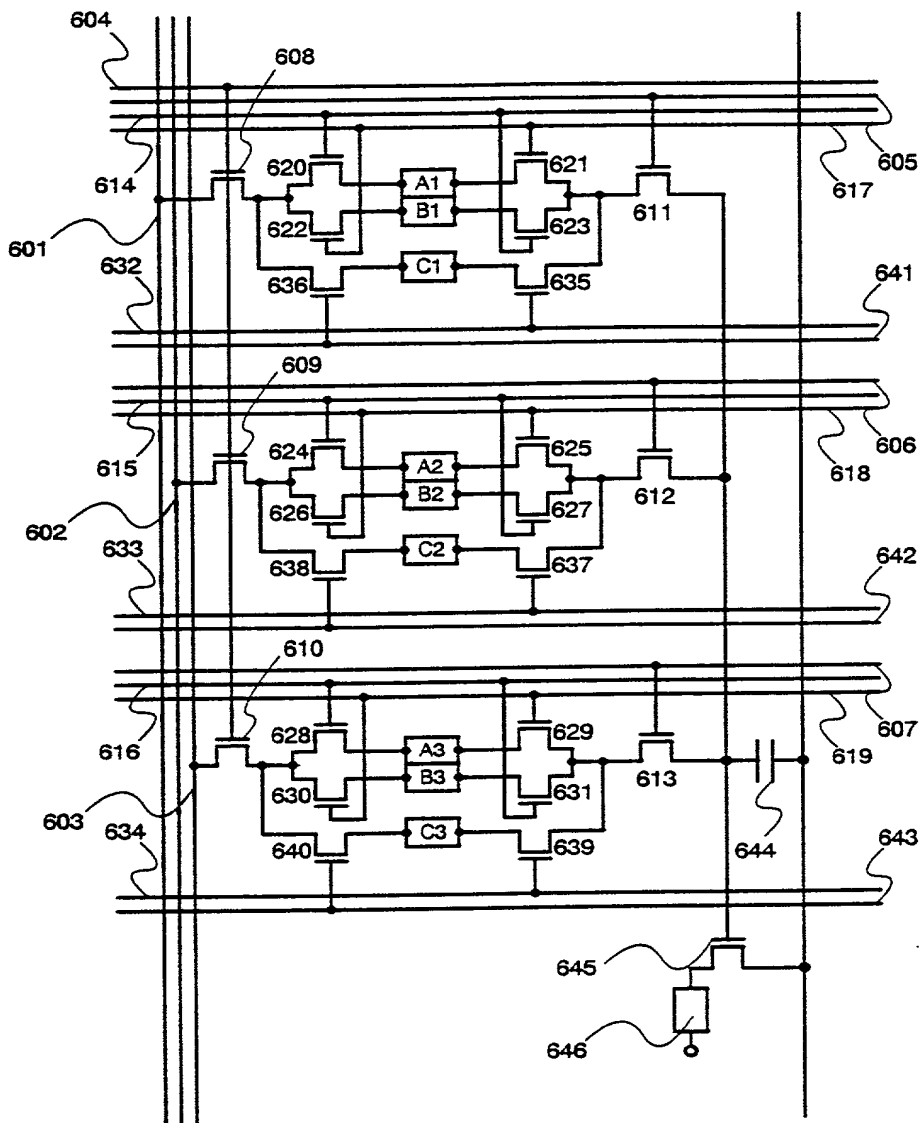


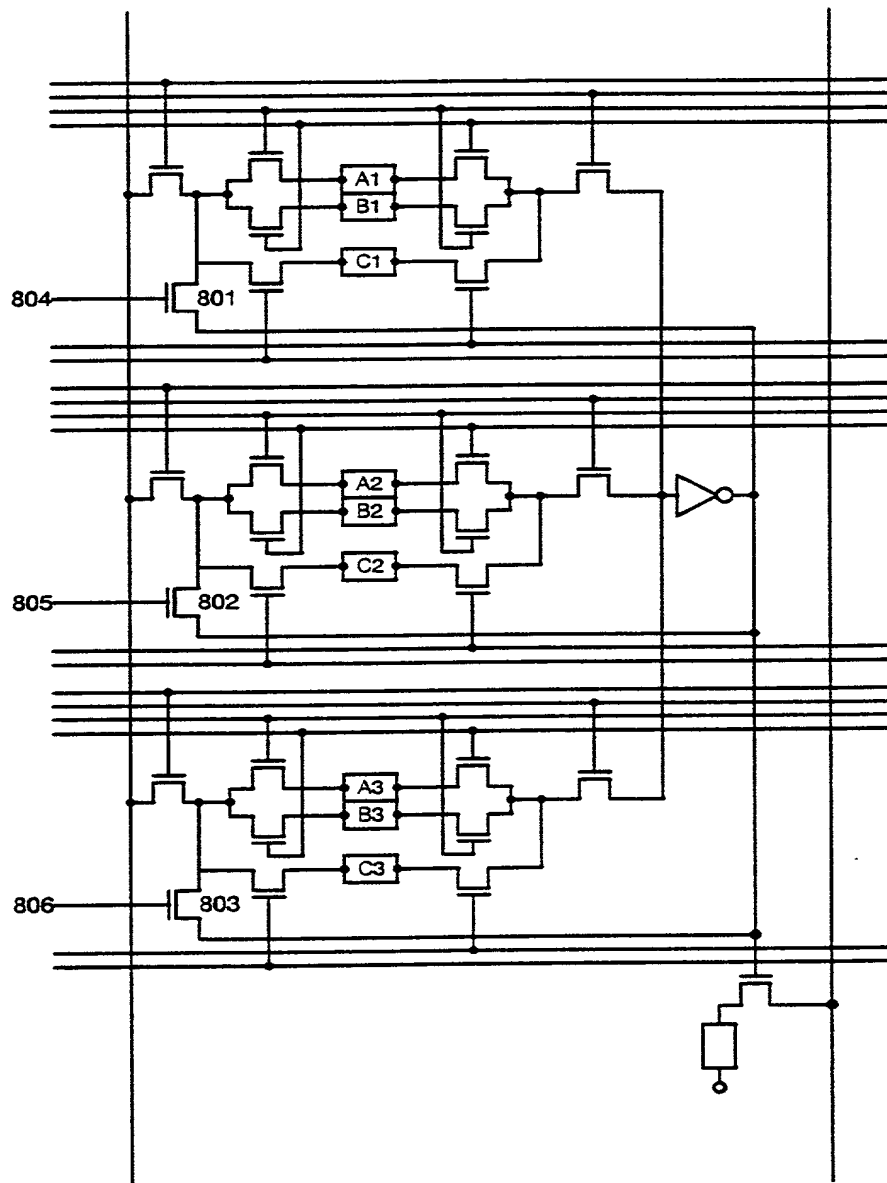
Fig. 5

Fig. 6

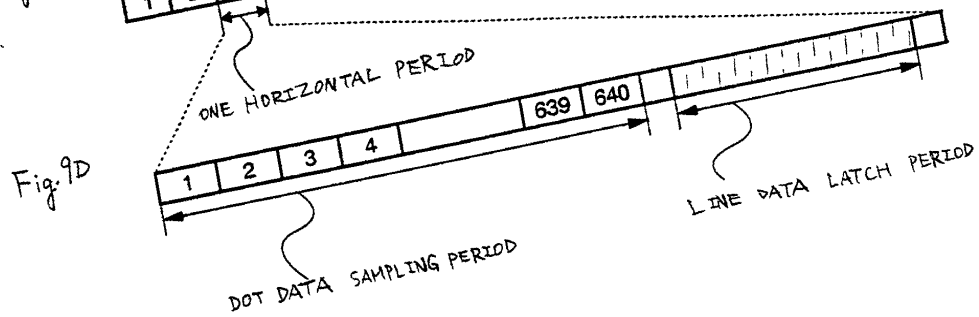
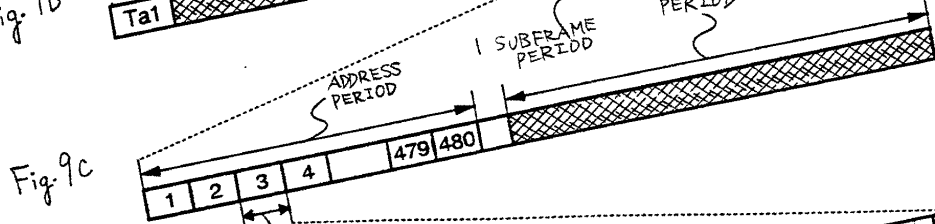
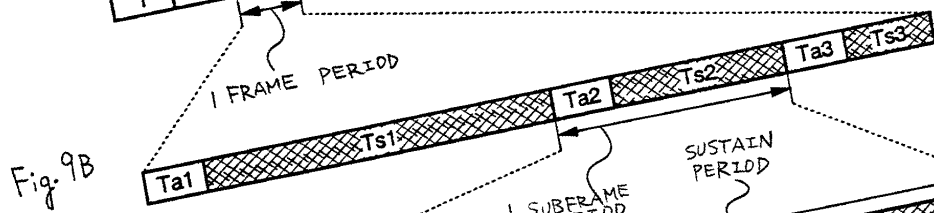
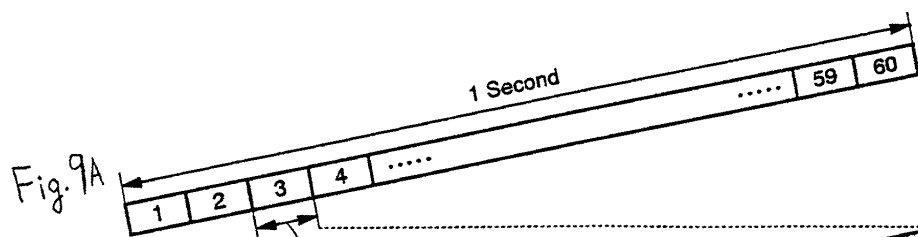


0001004-004704

Fig. 8



804~806 : REFRESHING SIGNAL LINE



FORMATION OF ISLAND-LIKE SEMICONDUCTOR FILM AND GATE INSULATING FILM
AND FIRST AND SECOND CONDUCTIVE FILMS FOR GATE ELECTRODE

Fig.10A

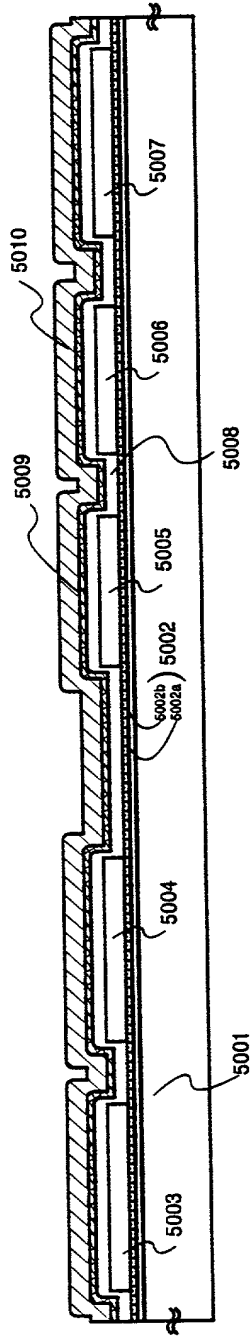


Fig.10B
FIRST ETCHING PROCESS
AND FIRST DOPING PROCESS

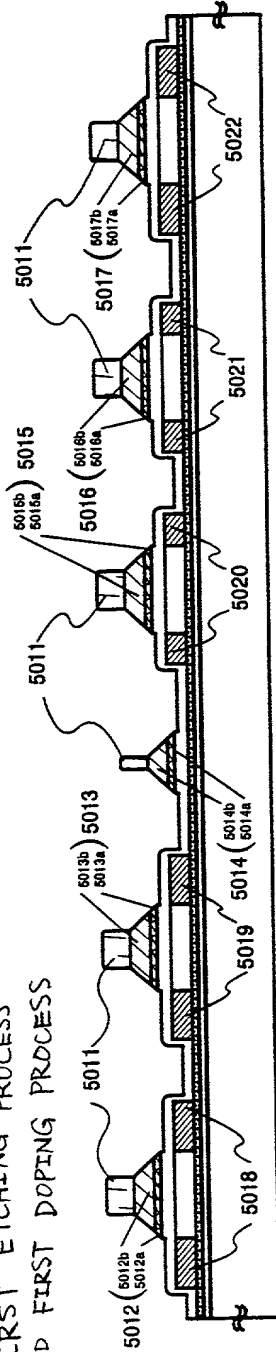


Fig.10C) SECOND ETCHING PROCESS

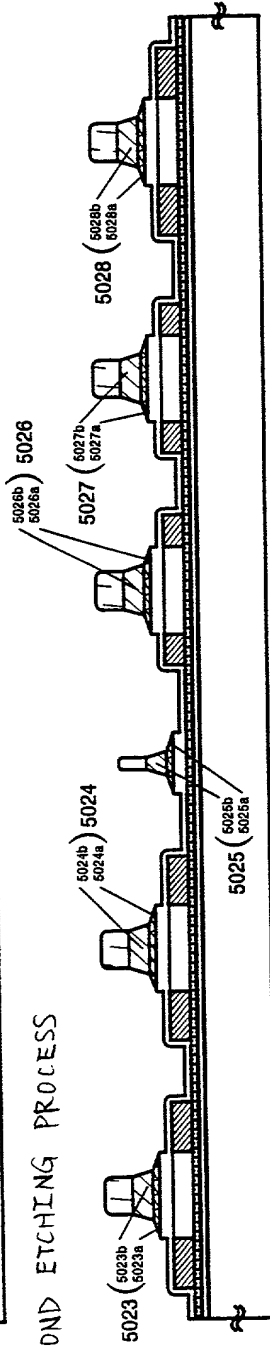


Fig. 11A SECOND DOPING PROCESS

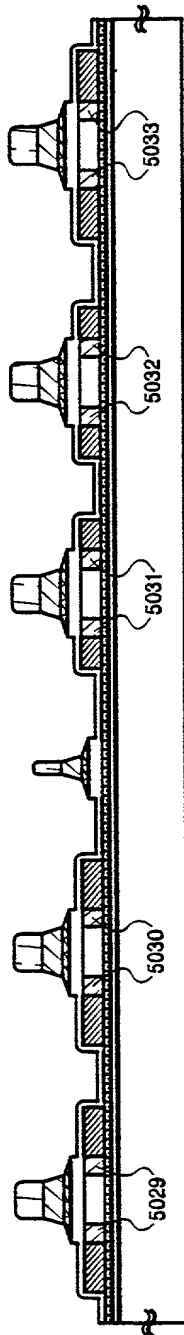


Fig. 11B THIRD ETCHING PROCESS

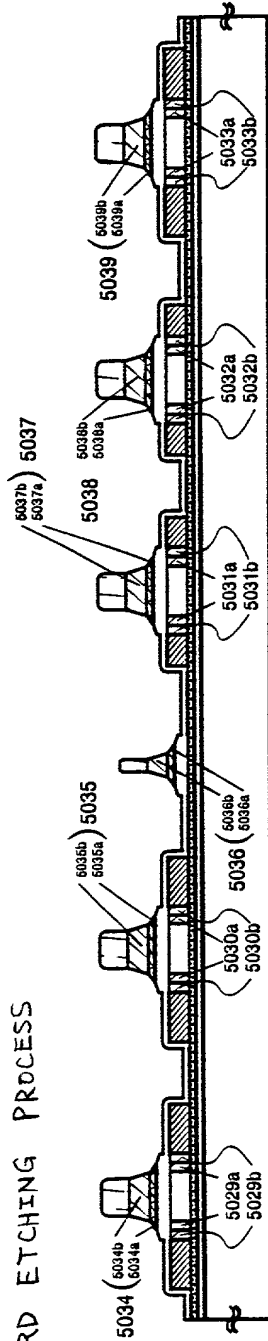
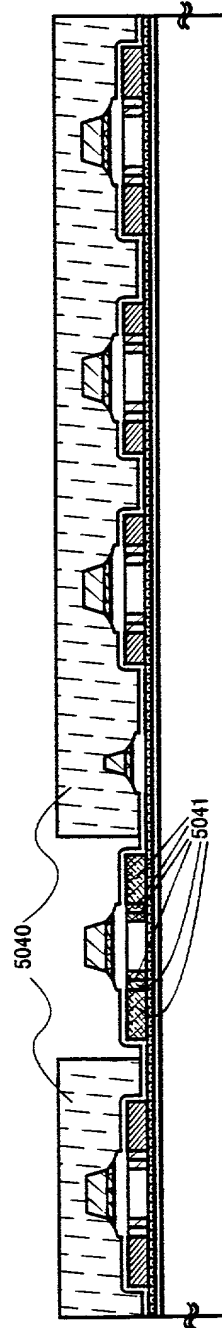
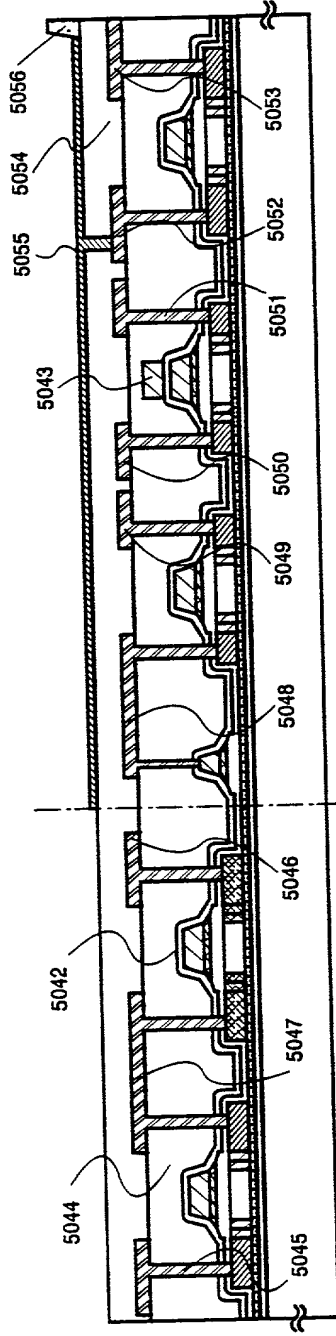


Fig. 11C THIRD DOPING PROCESS



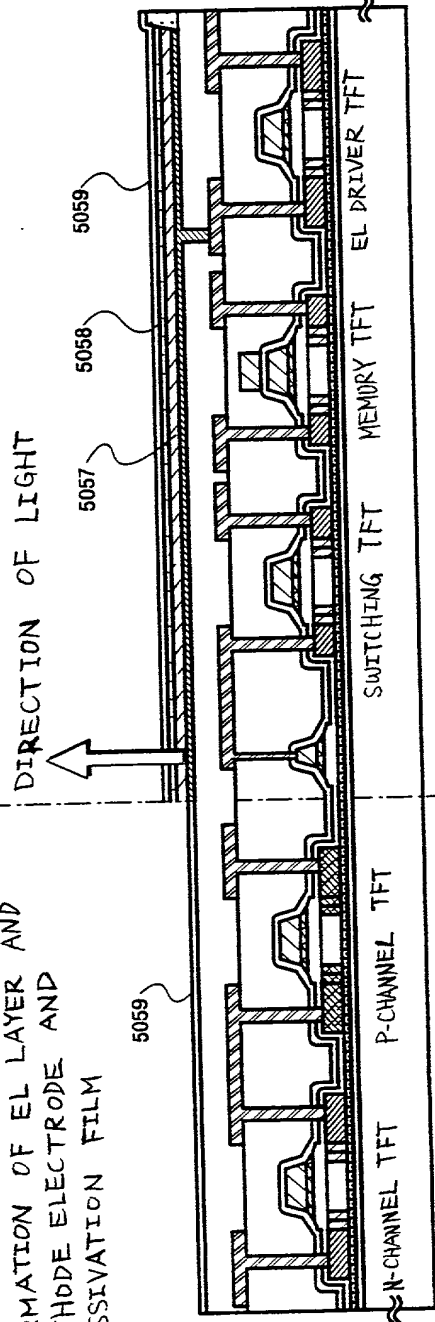
FORMATION OF SECOND GATE INSULATING FILM AND CONTROL GATE AND FIRST INTERLAYER INSULATING FILM AND WIRING AND SECOND INTERLAYER INSULATING FILM AND PIXEL ELECTRODE

Fig. 12A



FORMATION OF EL LAYER AND CATHODE ELECTRODE AND PASSIVATION FILM

Fig. 12B



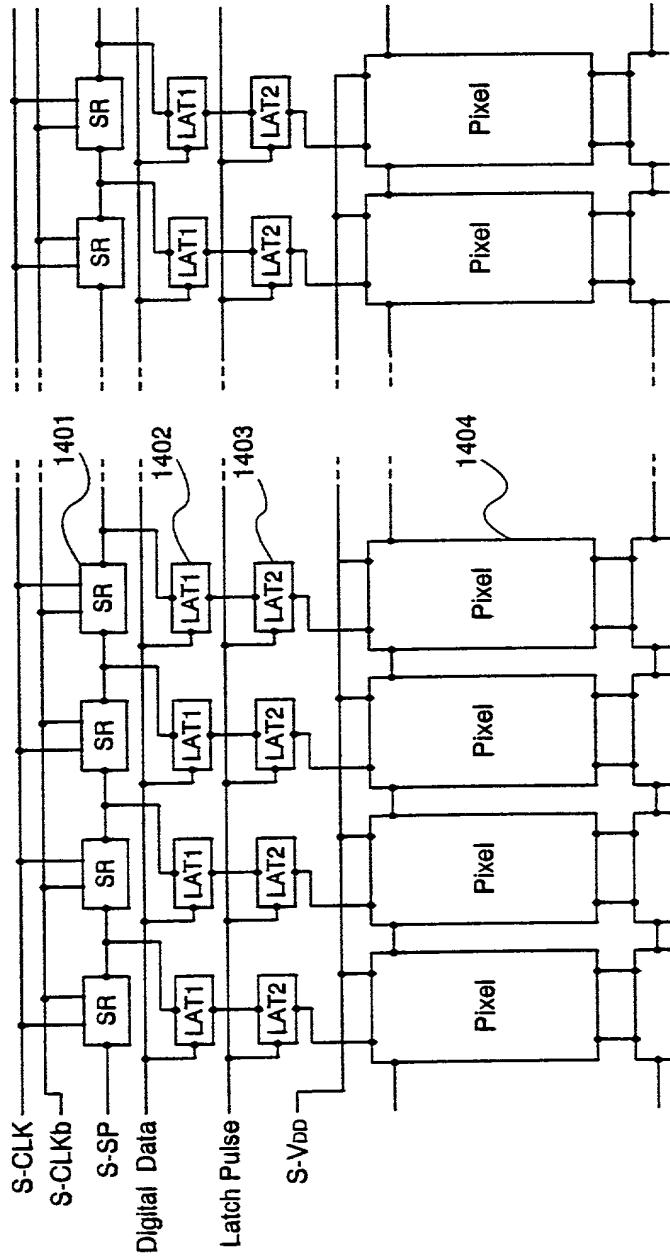
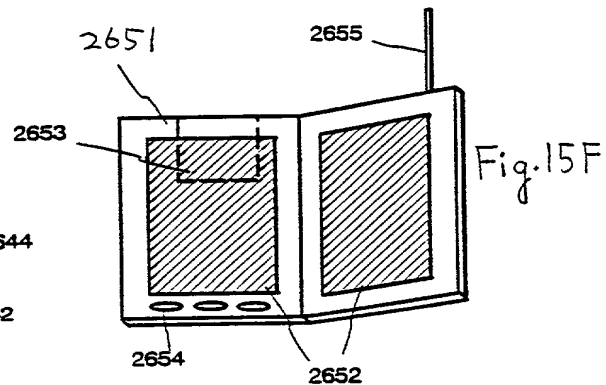
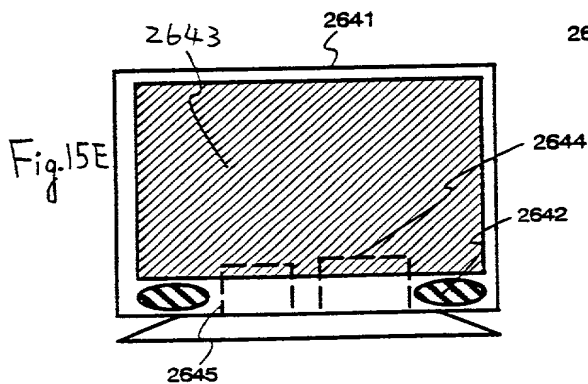
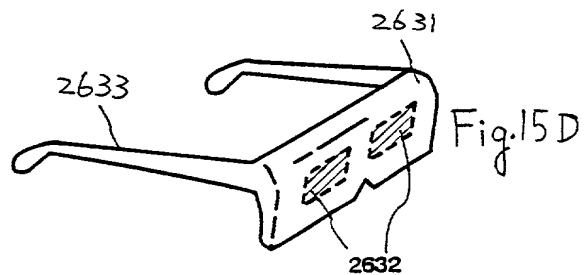
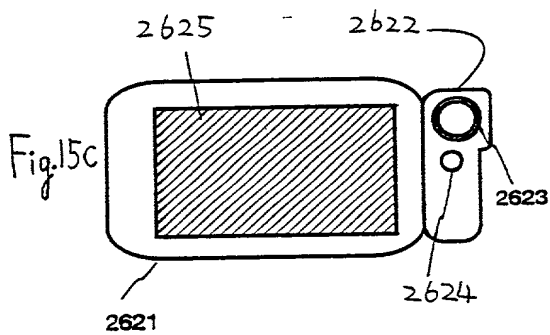
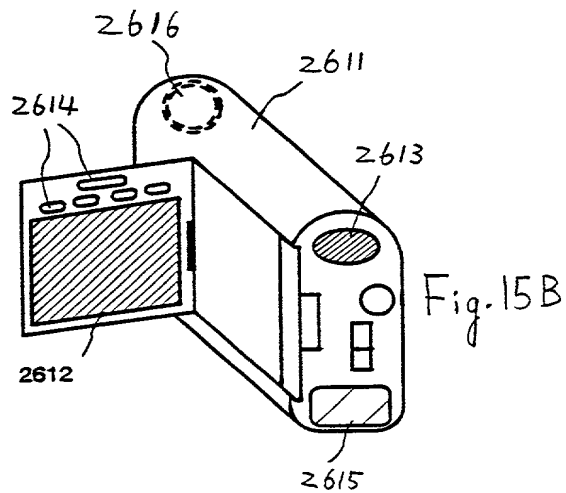
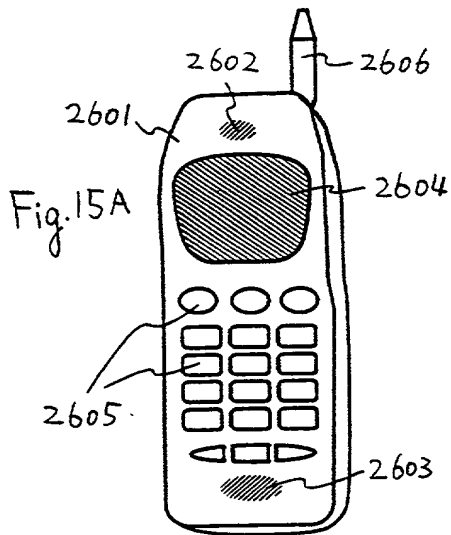
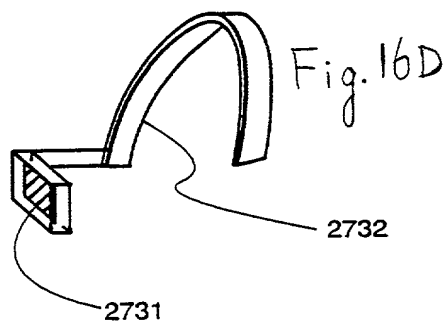
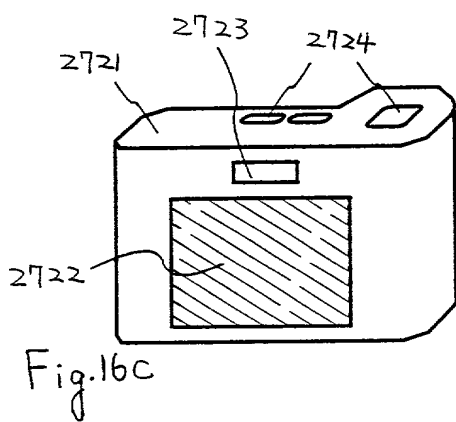
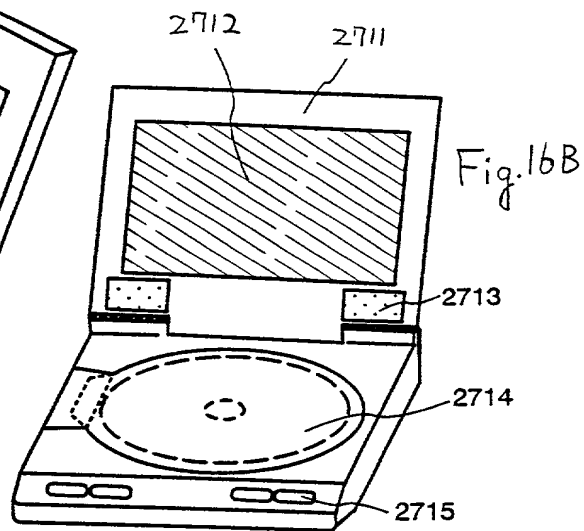
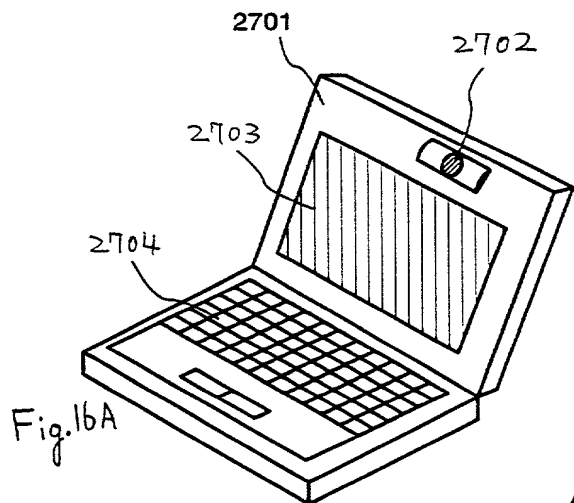


Fig.14





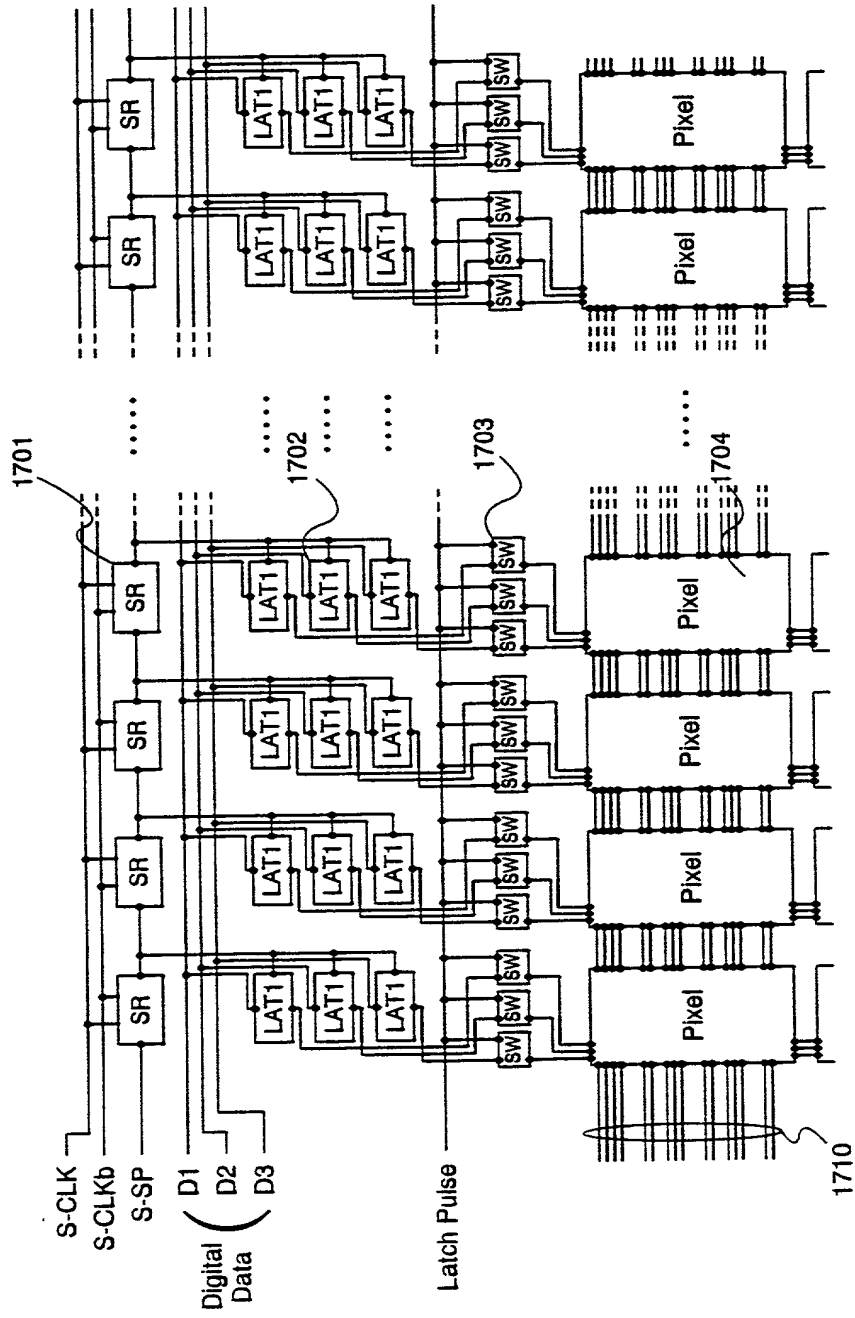


Fig. 17

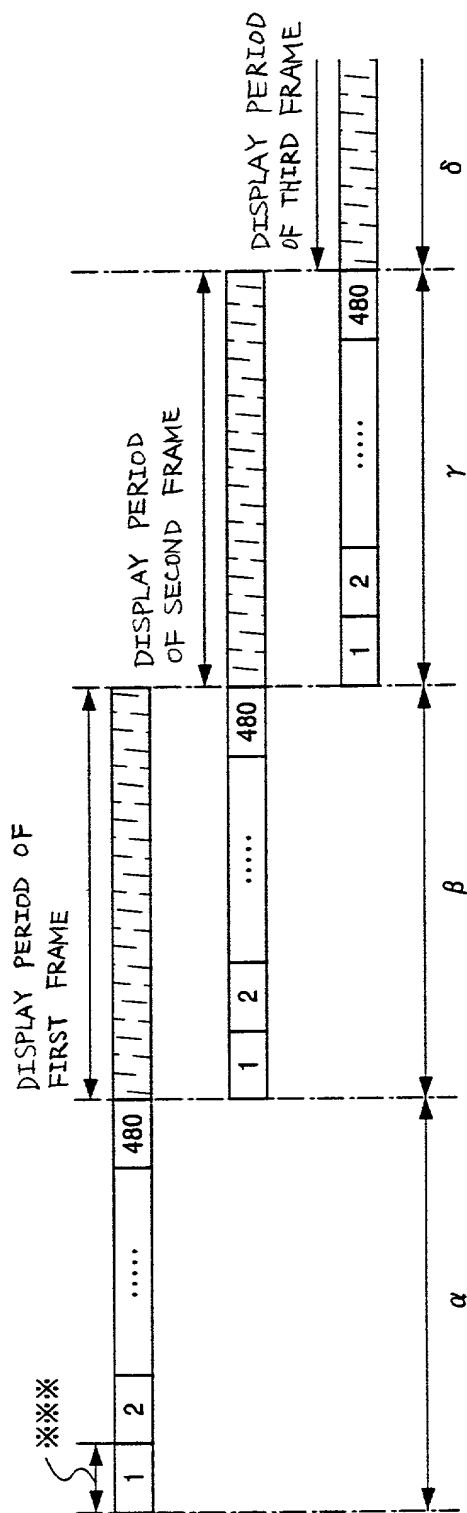


Fig. 18A

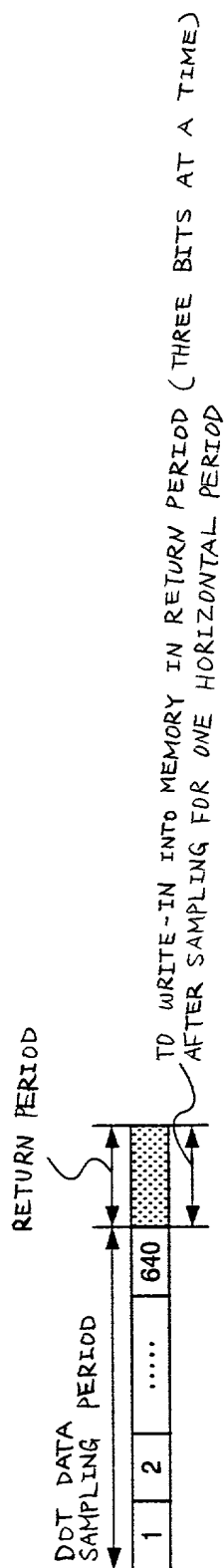


Fig. 18B

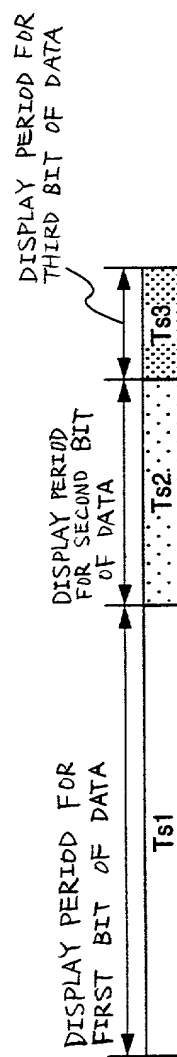


Fig. 18C

Fig. 19A

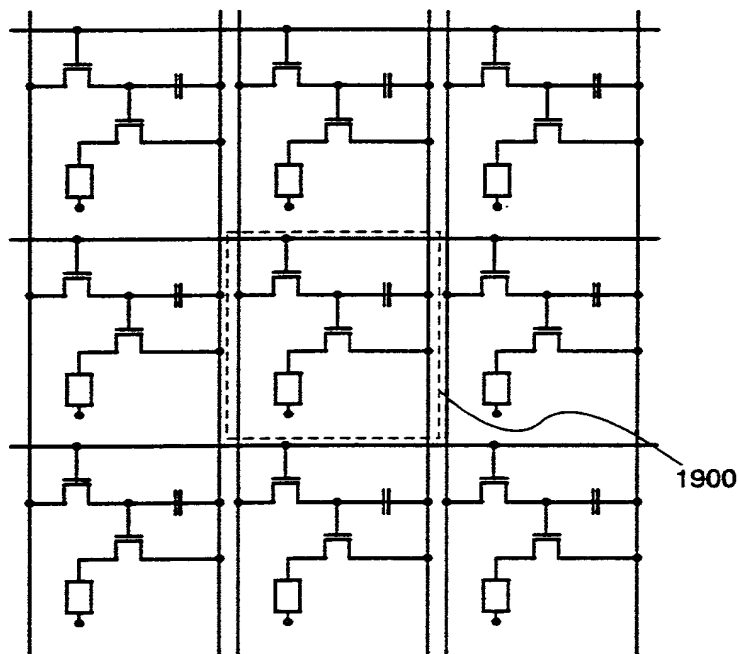


Fig. 19B

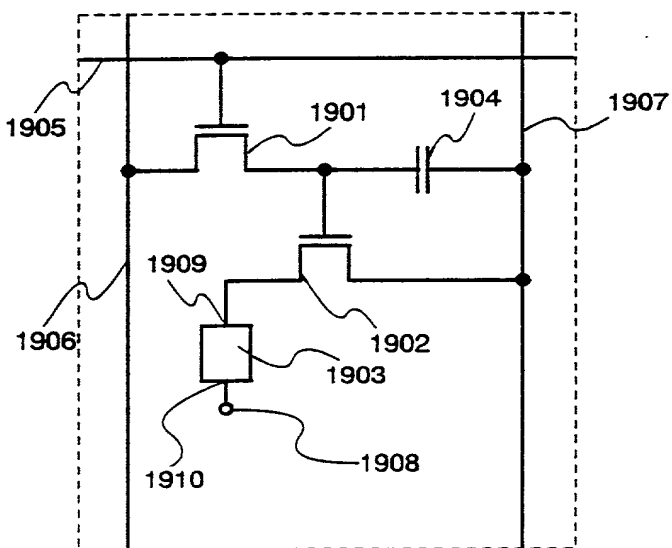


Fig. 20

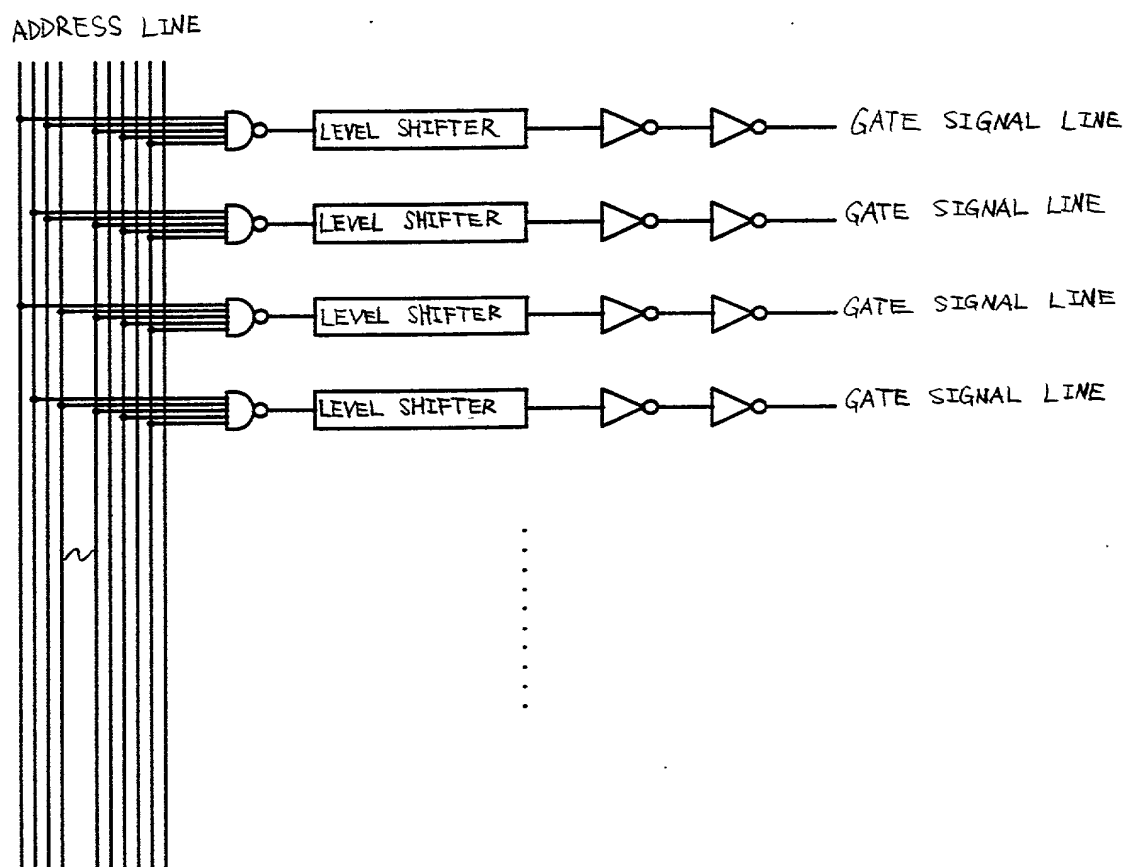
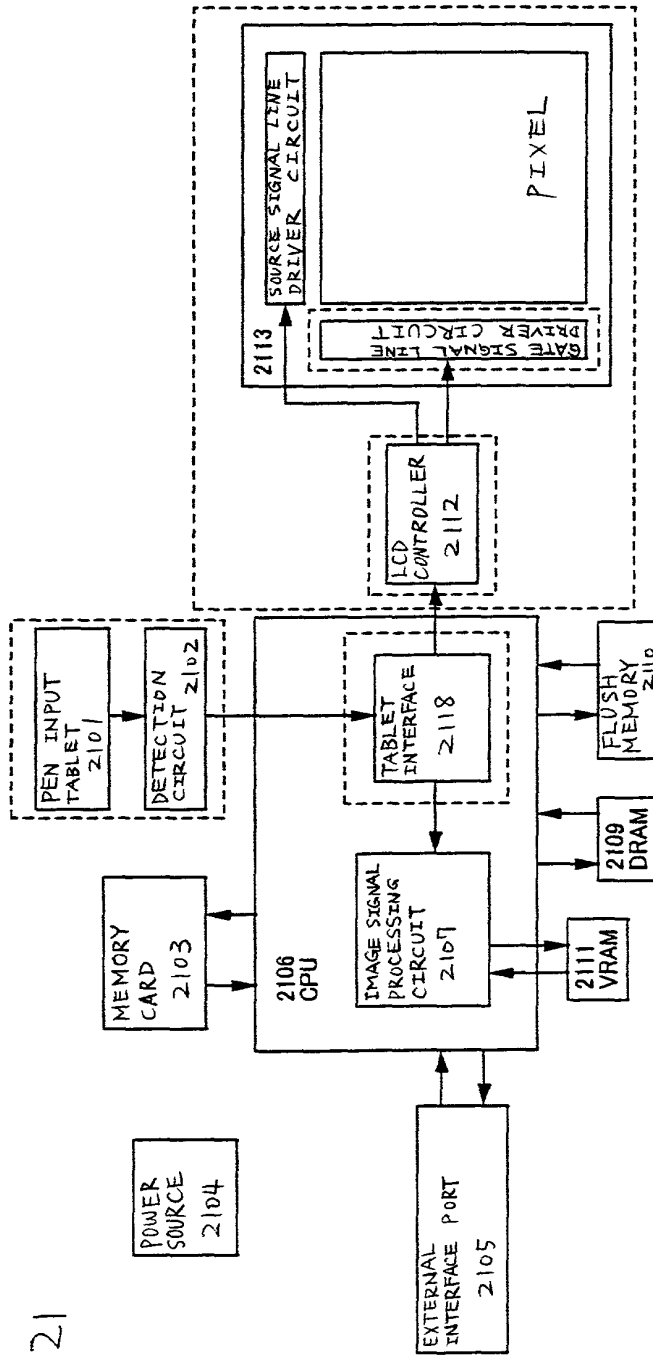


Fig. 21



BLOCK DIAGRAM OF PORTABLE INFORMATION TERMINAL

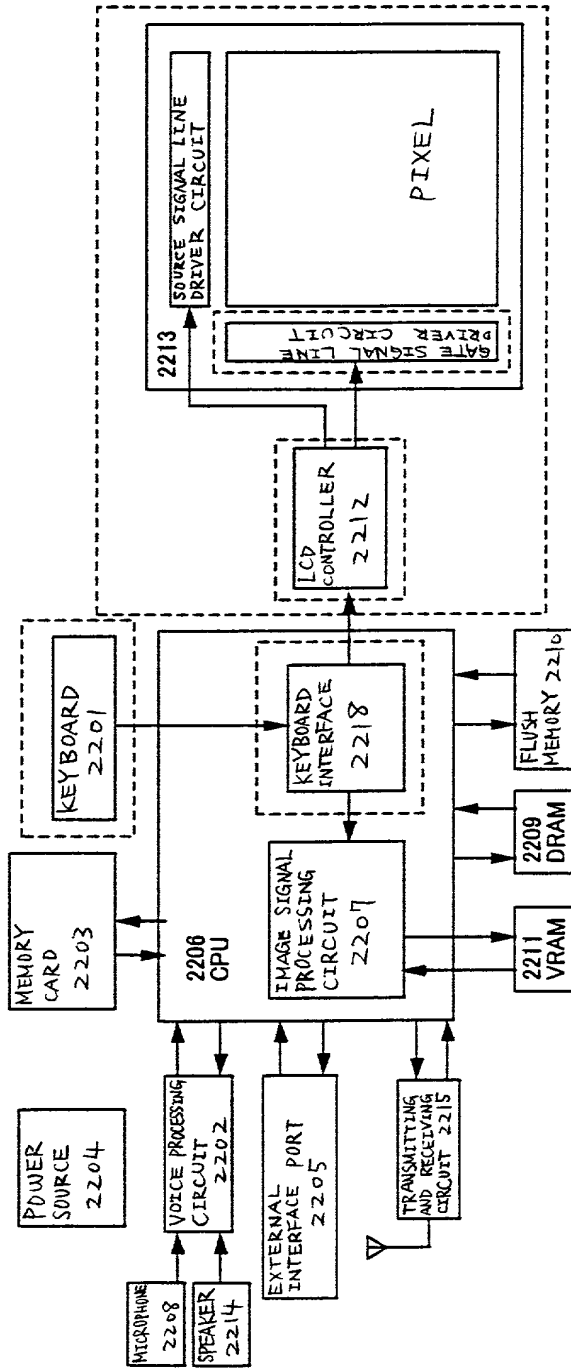


Fig. 22

BLOCK DIAGRAM OF MOBILE TELEPHONE

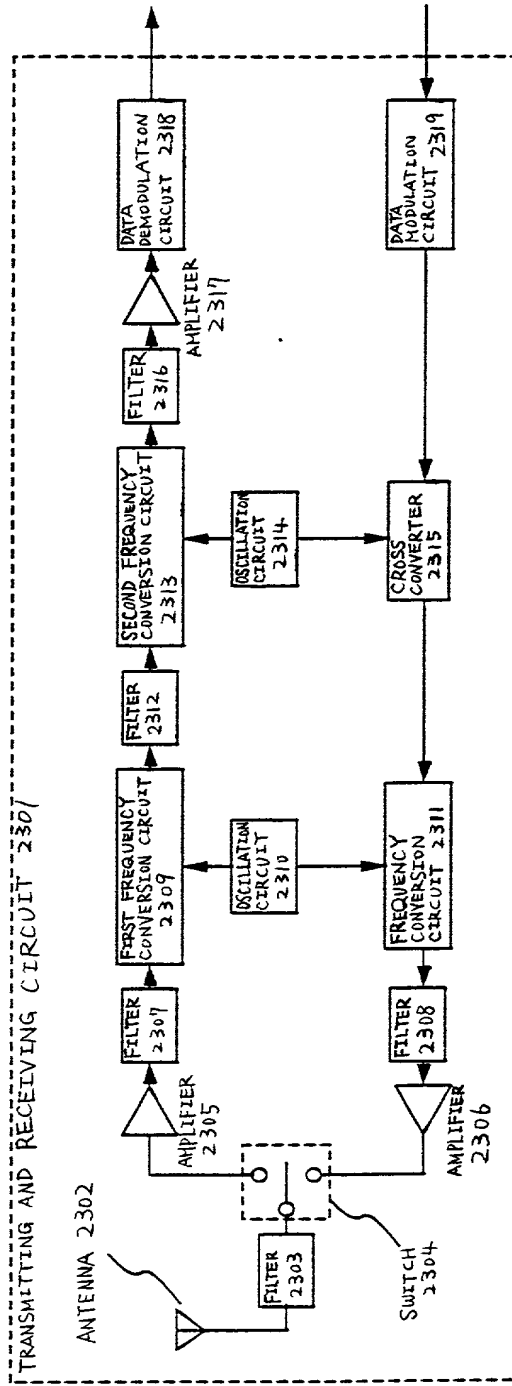


Fig. 23

BLOCK DIAGRAM OF TRANSMITTING AND RECEIVING CIRCUIT